

# Power Consumption in DFTs for OFDM Systems

Project Exam - Group 08gr1042

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APPLIED SIGNAL PROCESSING AND IMPLEMENTATION

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## Outline

### The Project (Jes)

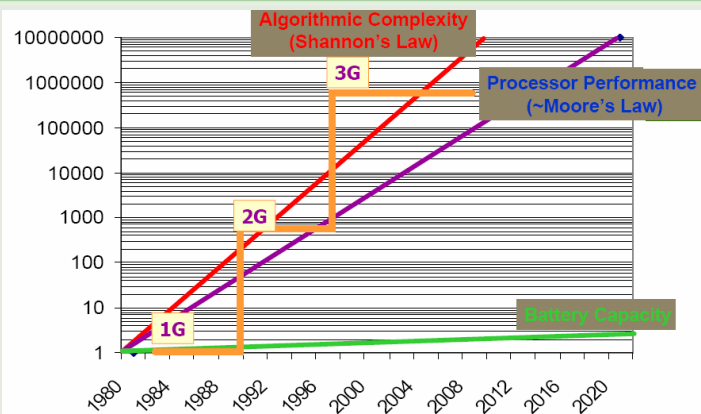
- 1 Motivation
  - Power and Mobile
  - OFDM and Transmission
  - Project Focus
- 2 Implementation
  - The Platform
  - FFT Algorithms
  - Design Choices
- 3 Results
  - Measured Results
  - Extrapolated Results
  - Conclusions

### Further Work (Peter)

- 4 Design Space Exploration
  - Potential Improvements
- 5 Design Revisions
  - Enable signals for ROM
  - SFFT Datapaths
  - Clock Generator
- 6 Resume

## Power and Mobile

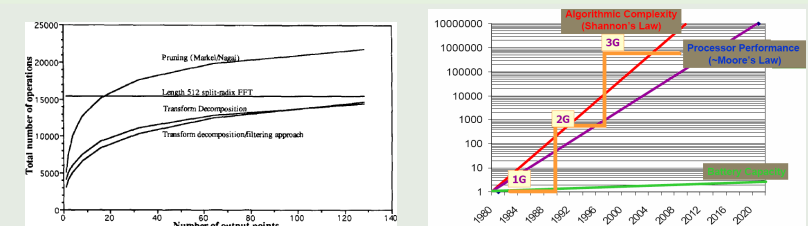
### An Illustration



From: <http://csdr.dk/>, SDR - An Agenda For Research (presentation)

## Moving to Mobile Architecture

### A Metric is Needed

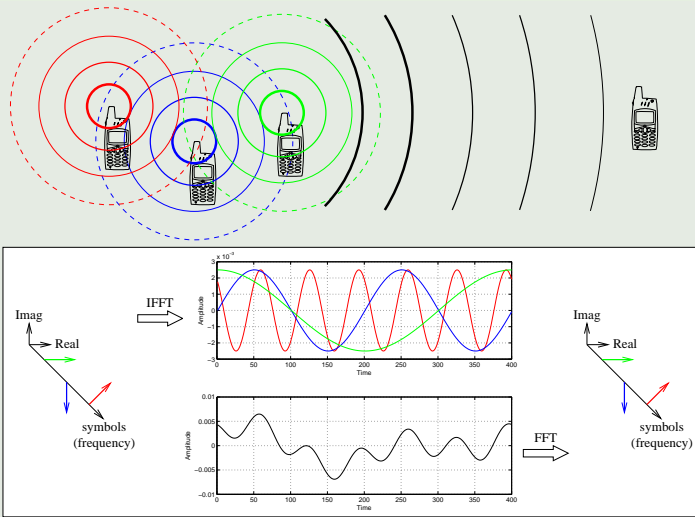


Left from: Soerensen and Burrus, 1993, "Efficient Computation of the DFT with Only a Subset of Input or Output Points"

Right from: <http://csdr.dk/>, SDR - An Agenda For Research (presentation)

# OFDM Transmission

## Orthogonal in Frequency

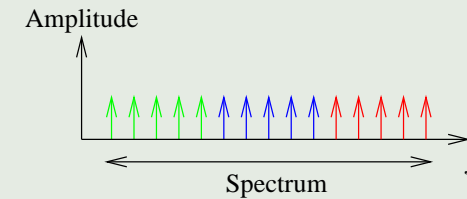


# Focus of the Project

## Problem Specification

*How well does the performance measure of computational complexity compare to power consumption in FPGA implementations of DFT algorithms for multiuser OFDM?*

## Frequency Selection

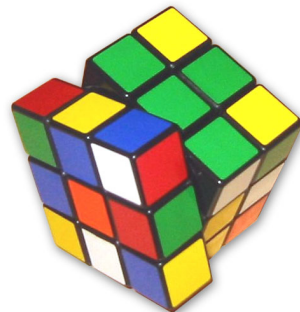


# Selected Platform

## FPGA

- Customizable Logic
- Scalable
- Designed for low-power applications
- Infinite Design Space

## Many Possibilities



From: ouferrat.blogspot.com

# The Possible Solutions

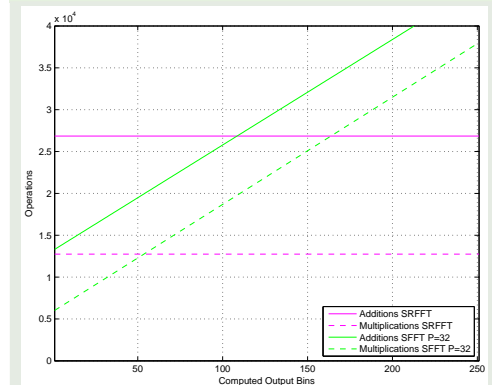
## Full FFT (SRFFT)

- Computes a full FFT
- Static
  - Execution Time
  - Execution Path

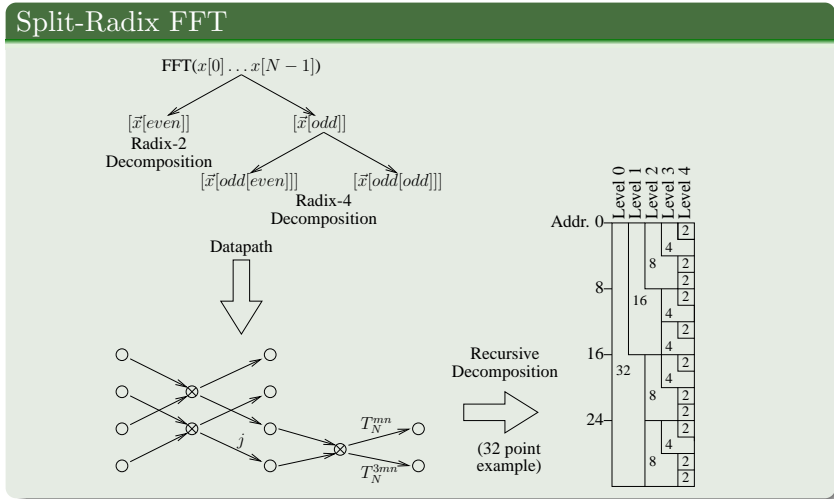
## Partial FFT (SFFT)

- Computes parts of an FFT
- Dynamic
  - Execution Path
  - Execution Time

## Computational Complexity



# Method 1: Full FFT



# Method 2: Partial FFT 1/2

### Sørensen FFT

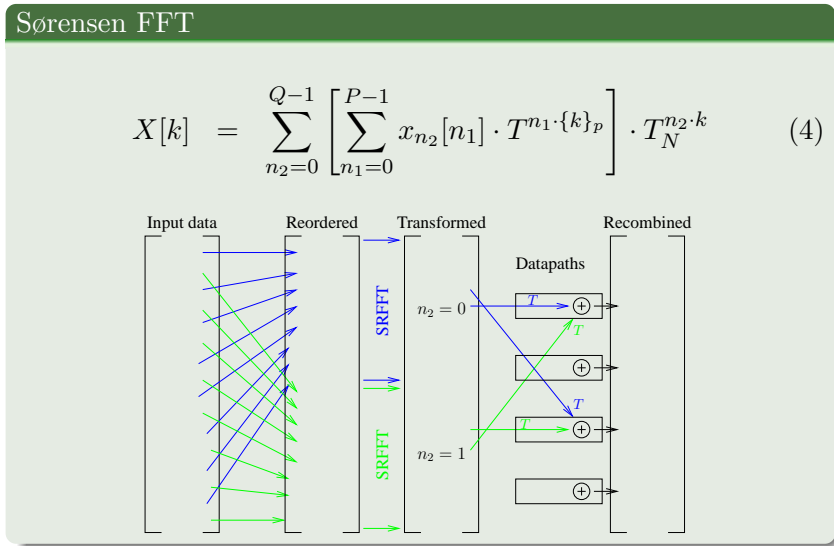
$$X[k] = \sum_{n=0}^{N-1} x[n] \cdot T_N^{n \cdot k}, \quad T_a^b = \exp\left(\frac{-2\pi j \cdot b}{a}\right) \quad (1)$$

$$X[k] = \sum_{n_2=0}^{Q-1} \left[ \sum_{n_1=0}^{P-1} x[n_1 \cdot Q + n_2] \cdot T_N^{n_1 \cdot Q \cdot k} \right] \cdot T_N^{n_2 \cdot k} \quad (2)$$

$$X[k] = \sum_{n_2=0}^{Q-1} \left[ \underbrace{\sum_{n_1=0}^{P-1} x_{n_2}[n_1] \cdot T^{n_1 \cdot \{k\}_P}}_{X_{n_2}[r] = \sum_{n_1=0}^{P-1} x_{n_2}[n_1] T_P^{n_1 \cdot r}} \right] \cdot T_N^{n_2 \cdot k} \quad (3)$$

$r = 0 \dots P-1, \quad r = \{k\}_P$

# Method 2: Partial FFT 2/2



# Resume

- ### What is Covered

  - Analysis of problem
  - Problem formulation
  - Implementations

### Results

  - Functional Verification
  - Power Usage
  - Power Usage vs. Computational Complexity

# Verification and SQNR

## SRFFT (Full FFT)

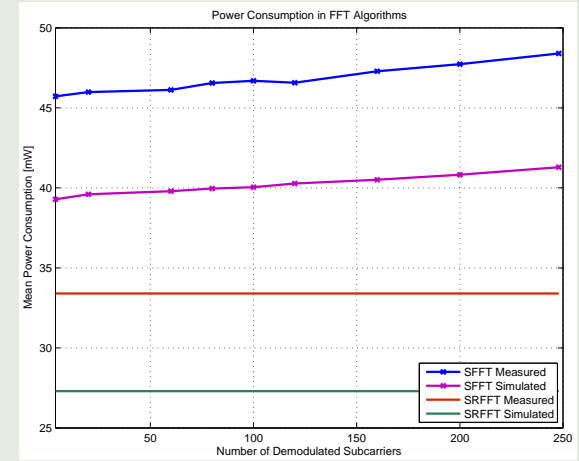
- Implementation shows SQNR of: 54.6 dB
- Loses approximately 4/13 fractional bits in implementation
- Implementation success

## SFFT (Partial FFT)

- Simulation shows SQNR of 52.2 dB
- Loses approximately 4/13 fractional bits in simulation
- Implementation provides wrong results

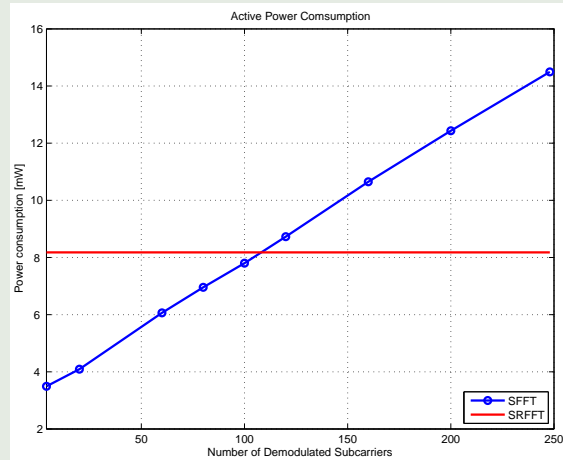
# Power Usages 1/2

## Project Results



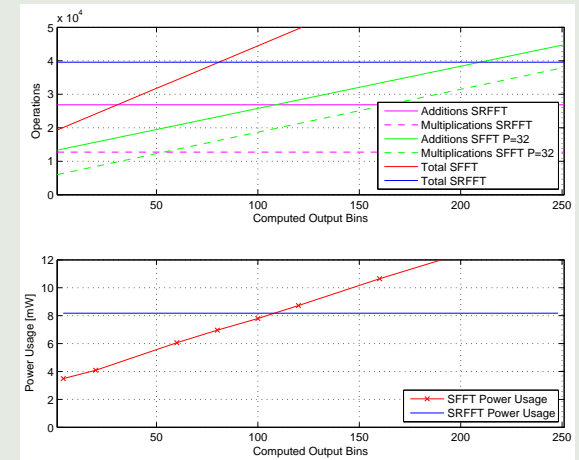
# Power Usages 2/2

## Assuming zero idle-Power



# Power Usages vs. Computational Complexity

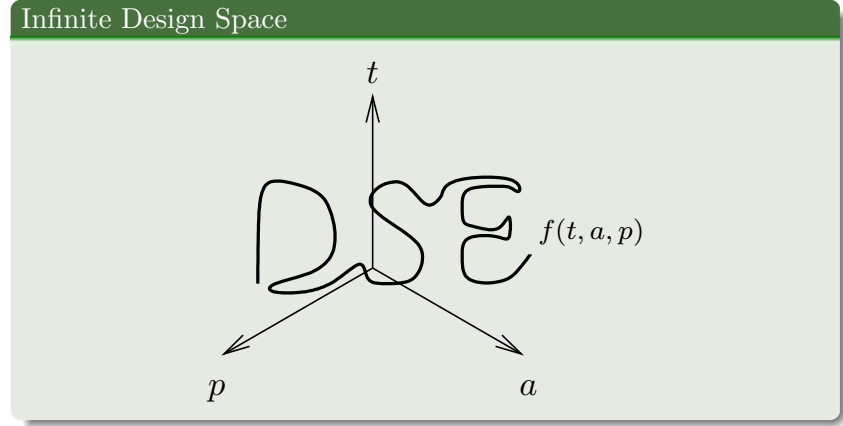
## Crossing Points



# Conclusions

- Functionally
  - Full FFT calculates correctly
  - Partial FFT needs more work
- Power-wise
  - Full FFT outperforms the Partial FFT
  - Assuming zero idle-power switches the roles
- Power vs. Computational Complexity
  - Assuming zero idle-power makes computational complexity somewhat accurate as a measure of power-usage.

# More Exploration?



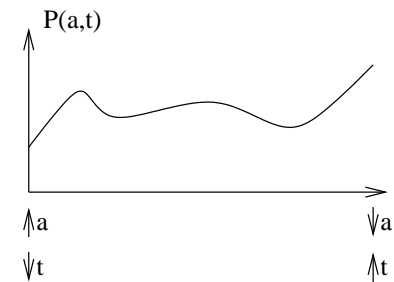
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# DSE

- Fucos Points
- Identification of high power consumpitons
  - Propose design improvements



## High Power Consumption Entities

- SFFT datapath
  - ROM lookuptables
- Clock generating PLL

### System Blocks Power Consumption

Group	Total	Dynamic	Routing
RAM # 1	1.91	1.35	0.56
Clock Generator	12.98	6.43	6.55
SRFFT	2.63	2.51	0.12
SFFT	10.89	10.01	0.88
Miscellaneous	4.30	4.30	0.00
Total	32.71 mW	24.60 mW	8.11 mW

## System Improvements

- Introduce enable / disable signal to LUTs
- Iterate over the number of instantiated SFFT datapaths
- Try out alternative clock generators

### System Blocks Power Consumption

Group	Total	Dynamic	Routing
RAM # 1	1.91	1.35	0.56
Clock Generator	12.98	6.43	6.55
SRFFT	2.63	2.51	0.12
SFFT	10.89	10.01	0.88
Miscellaneous	4.30	4.30	0.00
Total	32.71 mW	24.60 mW	8.11 mW

## Enable/Disable Signals for ROM

- Problem: LUTs are always active
- Solution: Use datapath enable signal to control LUTs

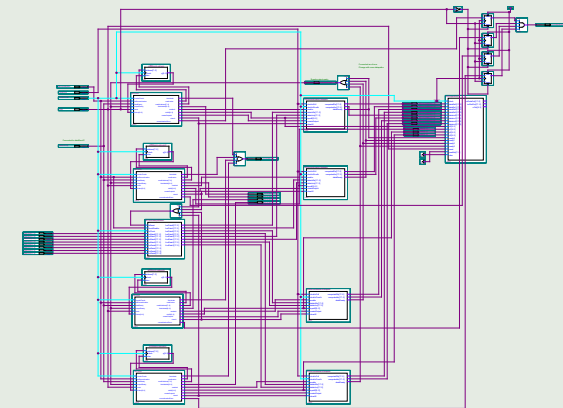
### Results

Entity	Before [mW]	After [mW]
2cos	1.21	0.15
ROMRe	0.60	0.11
ROMIm	0.30	0.06

## Number of SFFT datapaths

- Problem: 4 instantiations may not be power optimal

### SFFT Module



## Number of SFFT datapaths

- Solution: Conduct test with only one datapath for recombination

### Results

	4 Datapaths	1 Datapath
Main clock	32 MHz	100 MHz
Total Power	102.75 mW	129.24 mW
Dynamic Power	26.81 mW	44.67 mW
Static Power	66.39 mW	66.21 mW

## Clock generation using Counter

### Test Results

Voltage	Total [mA]		Dynamic [mA]		Static [mA]	
VCCINT	28.56	23.87	24.39	19.64	4.17	4.23
VCCA	18.43	22.76	0	2.19	18.43	20.57
VCCD	8.29	13.85	0	5.06	8.29	8.80

Blue = Counter    Black = PLL

## Clock Generator Revisions

- Problem: Clock generator responsible for significant system power consumption
- Solution:
  - Reduction of clock generator complexity by implementation with counters
  - Effects of circuit speed grade on PLL power consumption

### System Blocks Power Consumption

Group	Total	Dynamic	Routing
RAM # 1	1.91	1.35	0.56
Clock Generator	12.98	6.43	6.55
SRFFT	2.63	2.51	0.12
SFFT	3.71	2.81	0.90
Miscellaneous	4.30	4.30	0.00
Total	25.53 mW	17.40 mW	8.13 mW

## Effects of Device Speed Grade Settings

### Test Results

Voltage	Total [mA]		Dynamic [mA]		Static [mA]	
VCCINT	23.87	23.87	19.64	19.64	4.23	4.23
VCCA	22.76	22.76	2.19	2.19	20.57	20.57
VCCD	13.85	13.85	5.06	5.06	8.80	8.80

Blue = High Speed Grade    Black = Low Speed Grade

## Resume

### Project

- Computational complexity gives fair indication of power consumption if system is powered off when not calculating
- Design with potential power improvements

### Further Work

- Disable or power down inactive subsystems
- Utilize available area to reduce system clock frequency
- Counter implementation of clock generator

## The End

Thank You for Your Time

Questions?